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Improved protection scheme for shipboard microgrids based on high frequency impedance method with experimental validation

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ABSTRACT

This paper addresses the critical problem of fault detection in DC zonal shipboard microgrids, which is essential for ensuring system reliability and operational safety. The proposed method detects faults by utilizing the high-frequency characteristics of estimated impedance. The technique involves Fast Fourier Transform analysis of current and voltage waveforms to extract high-frequency components before and after a fault. These features help identify the system's high-frequency impedance via a communication system. Fault detection is achieved by comparing the estimated impedance with a predefined threshold. The performance of the method is evaluated using MATLAB/Simulink simulations and experimental implementations under various scenarios. Communication between components in the DC zonal microgrid is managed using the IEC 61850 standard. Results demonstrate the method's effectiveness in detecting faults under diverse conditions, including variations in fault resistance, dynamic load behavior, changes in photovoltaic irradiation, system configuration alterations, noise immunity, and multi-fault scenarios. The method achieves fault clearance times ranging from 0.17 ms in MATLAB/Simulink simulations to 33–45 ms in experimental tests, showing its capability to enhance fault detection in complex DC microgrid environments.

1. Introduction

The maritime industry is shifting towards shipboard microgrids (SMG) that minimize environmental impacts and optimize energy usage [1]. DC systems in SMGs offer numerous advantages over AC systems, such as reducing vessel size and weight by eliminating large transformers, straightforward integration of different power sources, no need for single-phase synchronization, and utilization of power electronics devices to handle disruptions and faults [2]. This has led to a growing trend toward using DC-SMGs in the maritime industry. Nonetheless, designing an efficient protection scheme for fault detection and location remains a significant challenge for DC-SMGs. Unlike AC systems, DC-SMGs lack a ground connection, making it difficult to identify line-to-ground faults due to the low fault current [3]. Additionally, pulsed loads requiring high transient power make it hard to quickly differentiate between normal and fault currents. Additionally, the small scale of SMGs can result in insignificant differences between short circuit impedances at various locations, making fault detection and location even more challenging [4].

In light of these challenges, additional precautions are necessary to ensure survivability, resilient power distribution, and reliability in DC-SMGs [5]. The protection methods applied to DC-SMGs can be divided into two categories: 1) Time domain measurement-based DC protections and 2) Frequency domain measurement-based DC protections, as previously described in the literature [6].

Time domain measurement-based DC protection methods can be categorized into two groups based on their communication requirements: non-unit protection, relying on data measured at the local end for fault detection, and unit protection, utilizing data measured at both remote and local ends [7]. Non-unit protection methods such as overcurrent protection, as discussed in [8], require a high level of expertise to set an appropriate threshold. In [9], reactors were integrated at the line terminals to establish a well-defined protected boundary, but this led to a decline in the efficacy of the control system

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and the efficiency of power transformation [7]. Unit protection schemes, such as differential protection and directional overcurrent in [10] and [11], require strict synchronization of data from both terminals [12].

In the frequency domain, the high-frequency component of the transient signal during a fault is used to detect faults accurately [13]. The active impedance estimation (AIE) method discussed in [14] and [15] estimated the system impedance by injecting a current spike and analyzing the high-frequency component of the transient voltage and current. However, this approach requires additional units and accurate calibration of the system impedance within a limited timeframe. The wavelet transform (WT) based method, discussed in [16] and [17], extracted the fault current signal at different frequency bands for analysis. However, this method can be computationally intensive and difficult to implement due to wavelet selections. The fault detection approach based on data clustering in [18] utilized short-time Fourier transform analysis to extract distinctive feature vectors of pulsed loads, allowing the differentiation between real faults and pulsed loads. A pilot-based distance protection scheme described in [19,20,21] applied Fourier transform on current and voltage measurements for estimating high-frequency fault transient impedance. Additionally, to guarantee the reliability and selectivity of the protection technique, permissive logic signals are employed according to the IEC 61850 communication standard. In conclusion, the overcurrent and directional protection schemes are mature and straightforward but may not be well-suited or suitable for ships with significant pulsed loads [22]. Meanwhile, computational constraints might be encountered by utilizing WT, AIE, and short-time Fourier transform (STFT) approaches [23]. A novel protection scheme is required for DC-SMG, which must maintain autonomy as they operate as islanded microgrids isolated from external resources.

This paper proposes a novel approach for fault detection in DC zonal SMGs based on the high-frequency characteristics of estimated impedance. The proposed method extracts high-frequency components from local and remote voltage and current measurements before and after a fault to determine the corresponding impedance, which is then used with impedance coordination to identify the fault location. The IEC 61850 communication protocol is implemented in the proposed method to transfer remote measurements. The proposed scheme is validated by designing a DC zonal SMG at MATLAB/Simulink. During normal operation, a Pole-Pole fault is simulated. The effectiveness of the proposed method is studied under different fault resistances ranging from 0.01 to 2 Ω. Two faults are simulated instantaneously to validate the robustness of the proposed method. To study the reliability of the proposed method, photovoltaic (PV) irradiation levels vary between 1000 and 200 $W/.m^2$. Moreover, a practical implementation of the proposed method is also introduced in which multiple faults at different locations are represented. Load variations and line outages considering line outages are also studied to validate the reliability and robustness of the proposed method.

The scope of this research focuses on the integration and performance of a fault detection mechanism for DC systems, offering insights into enhancing power system protection. The proposed method contributes to improving the design, reliability, and operational efficiency of modern electrical power systems, including microgrids. With microgrids playing a vital role in future energy systems, particularly in defense and specialized industries, this research supports advancements in fault localization and protection strategies, ensuring better performance and resilience for complex power networks. Table 1 shows a comparison between the recently published paper in the field of fault detection and localization techniques. The main contributions can be summarized as follows.

1. Proposing an innovative protection strategy for DC zonal SMGs utilizing high-frequency impedance estimation with integrating IEC 61850 communication protocol to enable precise transfer of voltage and current measurements across local and remote locations while ensuring synchronized timing.
2. Validation of the proposed approach through MATLAB/Simulink simulations involving a range of scenarios to establish its efficacy and accuracy.
3. Introducing a fault detection and localization method under diverse conditions, encompassing variations in fault resistance, dynamic behavior of generation sources and loads, changing the system configuration, and instances of multi-fault scenarios.
4. Implementing and validating the proposed scheme practically using a small prototype under different conditions, such as changing the fault locations, load variations, line outages, and impact of noise.

Table 1
Comparison between recent published papers for fault detection and localization techniques.

Ref.	Key Approach	Fault Types Covered	Communication Requirements	Computational Complexity	Noise Handling	Fault Location Accuracy
[24]	Multi-source information fusion with Bayesian networks	Low-resistance faults	Requires SCADA and PMU integration	High, due to data fusion and Bayesian networks	Limited	Moderate
[25]	Parameter estimation technique	Low and high impedance faults	Requires fast, synchronized communication	Moderate	Moderate	High for specific DC microgrid setups
[26]	Frequency-domain analysis with genetic algorithms	High-resistance faults	Requires fast data processing	High due to GA optimization	Limited	High for long transmission lines
[27]	WPT and neural network-based learning	High impedance and evolving faults	Requires two-end data synchronization	High due to complex learning algorithms	Sensitive to noise	High but dependent on noise conditions
[28]	Pattern recognition and linear discrimination	Grounding and three-phase faults	Requires wide area communication	High	Limited to clear patterns	Moderate
[29]	K-means clustering-based fault classification	Internal and external faults	Two-terminal data required	Moderate	Sensitive to new noise patterns	Moderate
[30]	Fault ride-through and blocking strategies	DC short-circuit faults	Requires ultra-fast communication	Moderate	Limited	High
[31]	One-terminal data-based fault location	Cross-circuit faults	Minimal	Low	Limited due to remote terminal noise	Moderate
[32]	Frequency analysis of traveling waves	Phase-to-ground and three-phase faults	Requires specialized recorders	Moderate	Limited	High for clean signals
Proposed Paper	High-frequency impedance-based fault location	Positive and negative pole-to-ground faults	Requires two-terminal data, but no synchronization	Low	Strong noise immunity with stable performance	High across different fault locations and noisy conditions

This paper is structured as follows: Section II describes the essential operation of the proposed protection scheme. Section III presents the simulation verification through MATLAB/Simulink by implementing different scenarios, and Section IV presents the experimental test bed setup. Finally, the conclusion of the paper is given in Section V.

2. Proposed SMG protection scheme

During DC faults, an immediate drop in voltage transpires at the fault location, accompanied by a surge in current. Consequently, the voltage and current can be perceived as a composite of high-frequency signals displaying distinct attenuation properties. The presented protective methodology capitalizes on this principle by extracting the high-frequency components of the voltage and current across the system to ascertain the transient high-frequency impedance of the system. This research introduces an innovative, intelligent electronic device (IED) tailored for DC zonal SMG, which integrates a high-frequency impedance estimation protection strategy to identify and pinpoint internal faults through comparative analysis of measured transient high-frequency impedances. Furthermore, communication signals aligned with the IEC 61850 standard are harnessed between both IEDs responsible for safeguarding the same line, thereby ensuring accurate fault isolation prior to transmitting tripping signals. These procedural stages are systematically structured within the framework of the proposed IED as follows.

A. Step 1: Measuring procedure.

In this step, the voltage and current are measured by sensors at each point in the system. Subsequently, the Fast Fourier Transform (FFT) is utilized in these measurements to extract the high-frequency component of each signal, according to [33].

$$F(x(n)) = \sum_{n=0}^{L-1} x(n) e^{-\left(i\frac{2\pi nk\Delta t}{L}\right)} \tag{1}$$

where n is the sample index, k is the frequency index, $L/\Delta t$ denotes the frequency steps, and x denotes the measurements taken.

B. Step 2: High-Frequency Impedance-Based Scheme.

The proposed scheme employs a communication-based protection scheme for DC zonal SMGs that utilizes high-frequency impedance estimation. The proposed impedance estimation scheme utilizes the principle that in case of a fault on the SMGs, the voltage at the fault point will suddenly decrease while the current will rise. This allows for precise fault location by estimating the impedance between the IED and the faulty point, as explained in [14] and [21].

A simplified circuit provided in Fig. 1 is used to examine faults in the system. Regardless of where a short-circuit takes place, the pole-pole fault is represented. $\boldsymbol{R_X}$ and $\boldsymbol{R_Y}$ are the equivalent resistance of the line from the relay point to the fault location, $\boldsymbol{L_X}$ and $\boldsymbol{L_Y}$ stand for the equivalent inductance of the line from the relay point to the fault location, and $\boldsymbol{R_f}$ signifies the fault resistance.

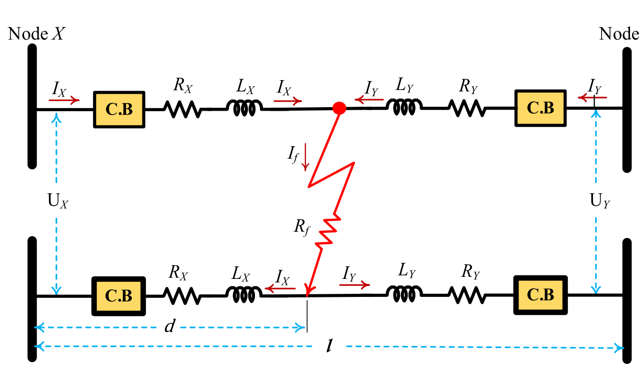


Fig. 1. Equivalent circuit diagram of the faulted network.

The equivalent resistance and inductance of the entire line, R_L and L_L, can be calculated before the occurrence of a fault as follows.

$$R_L = 2R_X + 2R_Y \tag{2}$$

$$L_L = 2L_X + 2L_Y \tag{3}$$

The calculation of the line impedance $\boldsymbol{Z_L}$ can be performed as;

$$Z_L = R_L + j\omega L_L \tag{4}$$

The impedance between node X and the fault point (Z) after the fault occurrence can be calculated as;

$$Z = 2R_X + j2\omega L_X \tag{5}$$

The high-frequency impedance estimation scheme can be determined using Kirchhoff's voltage law (KVL) as applied to the partial equivalent circuit shown in Fig. 1, as follows;

$$U_X = 2R_X I_X + j2\omega L_X I_X + I_F R_F \tag{6}$$

$$U_Y = 2R_Y I_Y + j2\omega L_Y I_Y + I_F R_F \tag{7}$$

where $\boldsymbol{U_X}$ and $\boldsymbol{U_Y}$ denote the high-frequency voltage components at nodes $\boldsymbol{X}$ and $\boldsymbol{Y}$, respectively, $\boldsymbol{I_X}$ and $\boldsymbol{I_Y}$ represent the corresponding high-frequency current components, and $\boldsymbol{I_F}$ represents the fault current.

Each device has local and remote readings with the voltage and current measurements exchanged between IEDs. The fault resistance can then be eliminated by subtracting the voltages at two nodes, resulting in calculating the voltage difference as:

$$U_X - U_Y = 2R_X I_X - 2R_Y I_Y + j2\omega L_X I_X - j2\omega L_Y I_Y \tag{8}$$

The equation in (8) can be simplified using (2) and (3), resulting in the following simplified formula:

$$\Delta U_{XY} = (I_X + I_Y)(2R_X + j2\omega L_X) - I_Y(R_L + j\omega L_L) \tag{9}$$

The equation in (9) can be simplified by utilizing (4) and (5) as follows:

$$\Delta U_{XY} = Z(I_X + I_Y) - Z_L I_Y \tag{10}$$

Therefore, the high-frequency impedance of network Z can be calculated by applying FFT to both the voltage and current signals, as shown below:

$$Z = \frac{\Delta U_{XY} + Z_L I_Y}{I_X + I_Y} \tag{11}$$

In the case of a pole-to-ground fault, the impedance along the line $Z_{L,PG}$ can be described as:

$$Z_{L,PG} = \frac{Z_L}{2} = \frac{R_L + jwl_L}{2} \tag{12}$$

The impedance between node X and the fault point (Z_{PG}) after a pole-to-ground fault becomes:

$$Z_{PG} = R_X + j\omega L_X \tag{13}$$

Applying KVL to the partial equivalent circuit for a pole-to-ground fault gives:

$$U_X = R_X I_X + j\omega L_X I_X + I_F R_F \tag{14}$$

$$U_Y = R_Y I_Y + j\omega L_Y I_Y + I_F R_F \tag{15}$$

The voltage difference between two nodes is expressed as:

$$U_X - U_Y = R_X I_X - R_Y I_Y + j\omega L_X I_X - j\omega L_Y I_Y \tag{16}$$

By substituting the line impedance for a pole-to-ground fault $Z_{L,PG}$ and using equations (12) and (13), the simplified formula becomes:

$$\Delta U_{XY} = Z_{PG}(I_X + I_Y) - Z_{L,PG} I_Y \tag{17}$$

Finally, the high-frequency impedance of the network can be estimated by applying the Fast Fourier Transform (FFT) to the voltage and current signals:

$$Z_{PG} = \frac{\Delta U_{XY} + Z_{L,PG} I_Y}{I_X + I_Y} \tag{18}$$

Therefore, the derived impedance is mainly influenced by the fault severity. By examining the estimated impedance data, short-circuit faults can be located as the imaginary part of the estimated impedance (reactance). So, it will not be affected by the fault resistance. Moreover, the same method can also be used to identify pole-to-ground faults as described in equation (18). Remote and local measurements of both ends need to be exchanged for calculating the high-frequency impedance of the line and comparing it with the pre-calibrated value. Moreover, the frequency of 1000 Hz was chosen for the high-frequency impedance-based scheme due to its suitability for capturing fault characteristics without interference from low-frequency harmonics. In standard power systems, harmonics are generally concentrated at multiples of the fundamental frequency (50/60 Hz). Operating at 1000 Hz ensures that the impedance response remains sensitive to fault events while avoiding noise from harmonics or operational disturbances. Additionally, frequencies significantly higher than 1000 Hz could introduce processing challenges, such as increased computational overhead and susceptibility to high-frequency noise, making 1000 Hz an optimal and practical choice as mentioned in [12,21]. A tripping signal will be generated to isolate the fault whenever the estimated impedance falls below the pre-calibrated threshold.

C. Step 3: Communication protocol based on IEC61850.

To implement the proposed scheme, process values of voltage and current from local and remote IEDs at the line terminals are essential. The information needs to be transferred as sampled values (SVs) from the transmitter of the remote IED to the receiver of the local IED over the ship's length, utilizing a wide area network (WAN). For this purpose, the IEC 61850 communication protocol is recommended in this study. IEC 61850 can be mapped onto specific protocols, like Ethernet, to facilitate the transmission of SVs and GOOSE (Generic Object-Oriented Substation Event) messages. In this paper, the proposed IED model incorporates SV messages mapped onto the Ethernet layer of the IEC 61850 standard based on the Open Systems Interconnection (OSI) model. Fig. 2 illustrates the mapping of various messages provided by the IEC 61850 over the OSI model. Specifically, Type 1A and Type 1 messages, such as Trip, Start, Close, Stop, etc., are time-sensitive GOOSE messages directly mapped onto the Ethernet layer to streamline the communication stack. On the other hand, Type-4 messages, which consist of raw data, represent continuous streams of synchronized data transmitted through Ethernet from digital instruments. The proposed IED utilizes SV and GOOSE messages that are transmitted directly to the Ethernet layer as a broadcast/multicast address. Type 2, 3, and 5 messages associated with American Customer Satisfaction Indexes (ACSI) applications, such as auto-control functions and file transfer messages, require message-oriented services and are time-tagged. For these types of messages, the Multimedia Messaging Service (MMS) protocol with Transmission Control Protocol/Internet Protocol (TCP/IP) stack is employed above the Ethernet layer [34]. Notably, SVs and GOOSE messages are exclusively used in the proposed IED. The proposed system follows IEC 61850 automation standards and comprises a Substation Communication Network (SCN) with similar IEDs. In the proposed IED, if a fault is detected by an IED at node X, a permissive signal S_X will be sent to the other terminal and vice versa for IED at node Y as it can send a permissive signal S_Y. Each IED send and receive a permissive signal, the tripping signal will be generated to isolate the fault instantaneously. Finally, a flow chart of the proposed method is illustrated in Fig. 3.

3. Simulation verification

The proposed adaptive protection scheme for Aquatanker vessel SMG parameters has been implemented and tested using MATLAB/Simulink®. The system consists of two DC buses powered by four sources: two batteries, PV, and a wind turbine. The system is divided into two zones with two loads, and each line is protected by two IEDs located at the beginning and end of the line, as shown in Fig. 4. Communication between the IEDs follows the IEC 61850 protocol. Table 2 provides system parameters. Various scenarios have been simulated to evaluate the system's performance as follows;

A. Scenario#1 Pole-pole fault during normal operation.
B. Scenario#2 Different fault resistances.
C. Scenario#3 Simultaneous faults.
D. Scenario#4 Change in generations.
E. Scenario#5 Load variations.
F. Scenario#6 Effect of a system contingency

A. Scenario#1 Pole-Pole fault during normal operation

A pole-pole (P-P) fault is introduced at point F1 at 0.5 s. The fault is located at the mid-point of the line during normal operation, as depicted in Fig. 4. Fault resistance is set at 0.0001 Ω. Fig. 5 illustrates the system voltage behavior during the fault event. The system voltage experiences a transient period at 50 ms, then returns to its nominal voltage once the fault is isolated. The currents of R1, load #1, and load #2 are displayed in Fig. 6. The load current is 40 A and returns to its steady state values after the fault is cleared. The clearing time in this test is 0.17 ms.

B. Scenario#2 Different fault resistances.

The proposed protection method's performance is assessed across various fault resistances to evaluate its effectiveness. A pole-pole (P-P) fault is introduced at 0.5 s, specifically located at 75 % distance from R5 at F2, as illustrated in Fig. 4. Multiple fault instances are generated with fault resistances ranging from 0.01 to 2 Ω. The estimated impedances observed by R5 for all faults, prior to issuing tripping signals to the

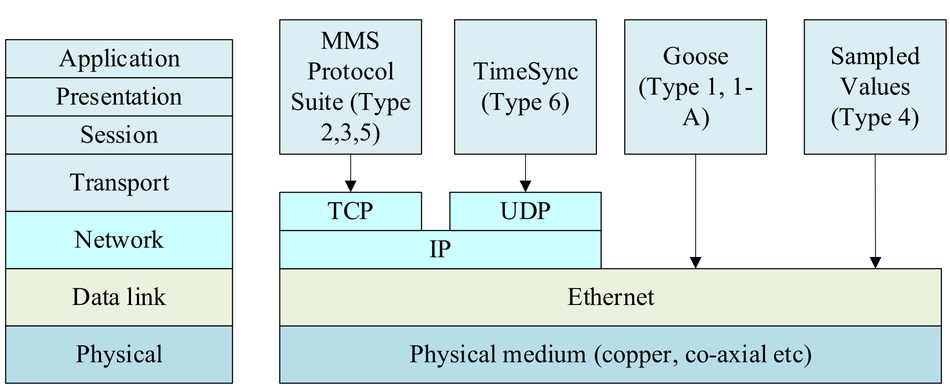


Fig. 2. IEC 61850 standard levels and service mapping in the ISO/OSI model.

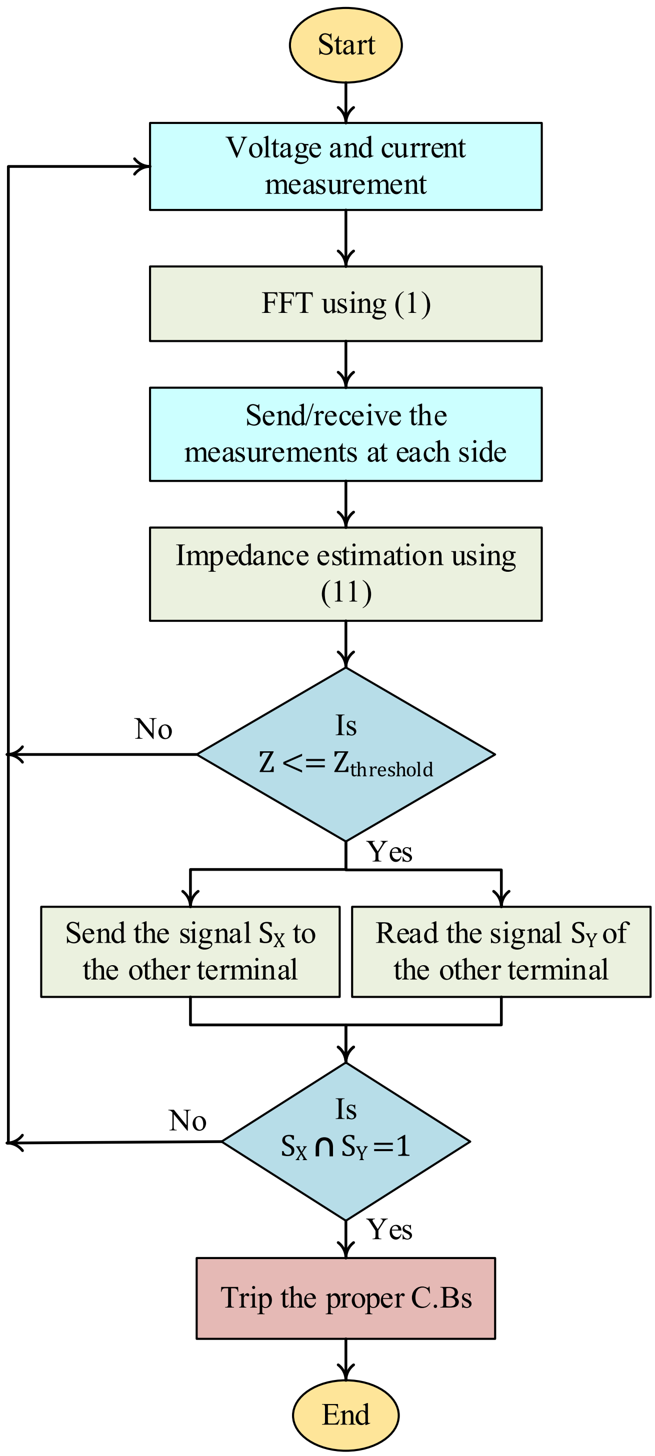


Fig. 3. Flow chart of the proposed scheme.

corresponding circuit breakers (CBs), are represented in Fig. 7. Notably, the measured impedance remains consistent regardless of the variation in fault resistance as the highest error is 5 % for 2 Ω making insignificant effect. This characteristic highlights the superior capability of the presented protection scheme in accurately identifying faults with diverse fault resistances.

C. Scenario#3 Simultaneous faults.

This particular scenario examines the performance of the suggested method under simultaneous fault conditions. Two pole-pole (P-P) faults, namely F2 and F5, occur concurrently on two separate lines. The first fault occurs between R5 and R6, while the second fault occurs between R13 and R14, as depicted in Fig. 4. The distances between the faults F2 and F5 from R5 and R14, respectively, are set at 15 %. Both faults are initiated at t = 0.5 s with a fault resistance of 0.0001 Ω. The variation in system voltage throughout the fault duration is illustrated in Fig. 8. In contrast, the currents in the system's lines and loads are presented in Fig. 9. Notably, R5, R6, R13, and R14 are exclusively tripped by their corresponding circuit breakers, showcasing the robustness of the proposed method when dealing with simultaneous faults.

D. Scenario#4 Change in generations.

The suggested scheme's performance is influenced by the fluctuating PV irradiation levels in the integrated system, particularly when high PV penetrations are present. This scenario investigates and assesses the impact of these variations on the proposed scheme. A pole-pole (P-P) fault is intentionally introduced at the mid-point of the line, specifically at F4, as depicted in Fig. 4. The fault resistance is set at 0.0001 Ω. Multiple fault occurrences are simulated while altering the PV irradiation levels, ranging from 1000 to 200 W/m^2 The depicted impedances for R12 can be observed in Fig. 10. Remarkably, it can be observed that the estimated impedance remains consistent irrespective of the changes in PV irradiation.

E. Scenario#5 Load variations.

Load fluctuations necessitate redefining the conventional protection thresholds due to alterations in line power flow impacting measured impedance. These established methods cannot differentiate between abrupt load current changes and fault currents. To ascertain the efficacy of the proposed approach in load variations, this scenario is considered where the load at zone#1 decreases by 25 % and the load at zone#2 increases by 25 %. A P-P fault is introduced with a 0.0001 Ω fault resistance along the line connecting R11 and R12, positioned 37 % away from R12. Fig. 11 depicts the system voltage variance during these load changes, while Fig. 12 presents the currents across system lines and loads. Notably, the load fluctuations do not impact the estimated impedances acquired by R11 and R12.

F. Scenario#6 Effect of a system contingency.

In this scenario, a P-P fault is introduced at F3, located midway between R9 and R10, as shown in Fig. 4. The fault is replicated twice: once with the line connecting R1 and R2 and once without it. The fault, occurring at 0.4 s, features a fault resistance of 0.0001 Ω. Fig. 13 visualizes the system voltage variation for both scenarios, while Fig. 14 depicts the currents within the system's lines and loads when the R1-to-R2 line is absent. Remarkably, the proposed method remains unaffected by the line outage, as it solely relies on the line impedance rather than the entire system impedance.

G. Scenario#7 The impact of noise.

In this scenario, to assess the impact of noise on the reliability of the proposed method, different noise levels were applied to the voltage and current signals. In this study, 30 dB band-limited white noise was introduced into the voltage and current signals measured by R5. A pole-to-ground fault was simulated at F2, specifically located at 75 % distance from R5, as illustrated in Fig. 4. The captured signals of current are shown in Fig. 15 with 30 and 50 dB signal to noise ratio (SNR). The simulation results reveal that variations in the signal-to-noise ratio (SNR) have minimal effect on the proposed method's accuracy, confirming that the proposed method effectively maintains accurate impedance estimates even under significant noise conditions.

4. Hardware validation

A DC zonal SMG prototype was built to validate the accuracy of the proposed protection scheme in a practical setting, as shown in Fig. 16. The system has two DC buses fed by two power supplies to supply power to the electrical loads. The emulation of the lines is achieved by employing inductors of 6 μH and resistors of 5 mΩ. In that construction, the first line will be protected by two relays and two smart meters, facilitating communication through Modbus TCP/IP. The relays and smart meters are all connected to the Acti9 SmartLink. Acti9 Smartlink is

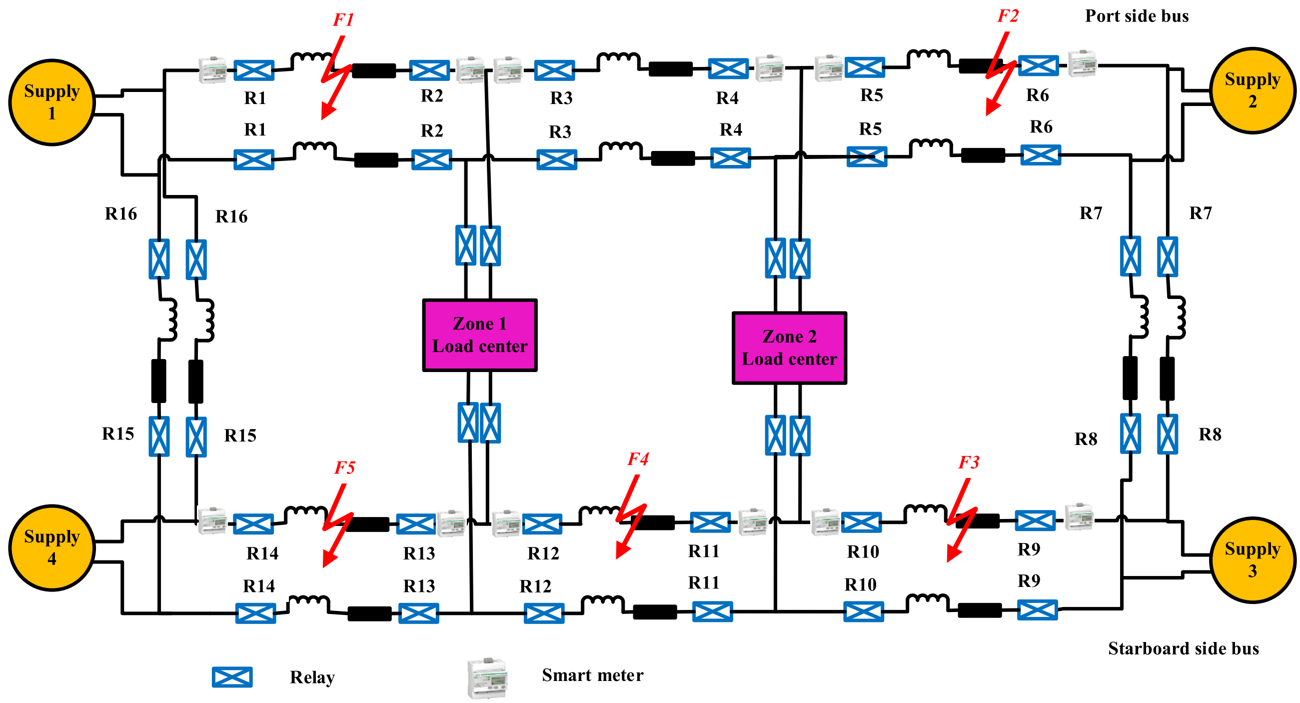


Fig. 4. Structure of the proposed DC zonal SMG.

Table 2
The system Parameters.

Parameter	Value
Ship length	400 *m*
Ship width	31 *m*
Resistance per unit length	0.32×10^{-6} Ω/m
Inductance per unit length	0.17 μH/m
Fault resistance range	0.0001–2 Ω
Load zone 1	40 kW
Load zone 2	40 kW
Rated DC voltage	1 kV
Solar cell (G3)	96.3 kW
Wind turbine (G4)	5 kW
Battery (G1, G2)	

a smart communication module designed to enable remote monitoring, control, and data collection for the connected electrical devices by 7 and 11 channels according to the device number [35]. The proposed method and fault location using high-frequency impedance estimation results are experimentally validated in a small prototype consisting of one zone.

The technical specifications of all devices used in the system can be found in [35]. The components installed in this experiment are depicted in Fig. 17 and can be grouped into the following subsystems:

- *Industrial Control and Supervision System:* Including the PC as a controller depending on Visual Basic programming language implemented at Visual Studio Software.
- *Protection System:* Featuring smart meters and relays connected to Acti9 SmartLink.
- *Communications System:* Modbus TCP/IP communication protocol and Ethernet cable.

In this context, the relays isolate the fault and are connected to the line terminals. The SCADA system also collects data from smart meters. The construction of the smart meter involves the integration of the ZMPT101B voltage sensor, the ACS712 current sensor, and the Arduino platform. These components work together to measure voltage and current and transmit the data to the PC for display and remote access by the user. Acti9 Smartlink is used to distribute the tripping signals to all relays in the system and collect the data from smart meters in the system.

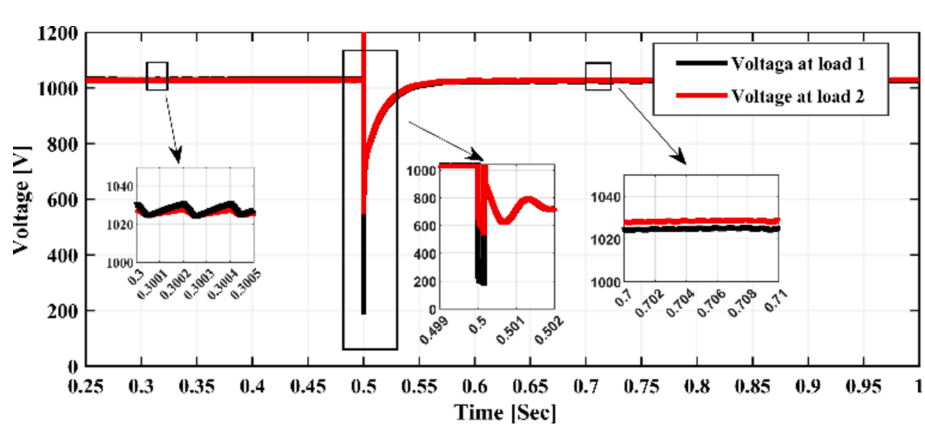


Fig. 5. System voltages during P-P fault at F1 (at t = 0.5 s).

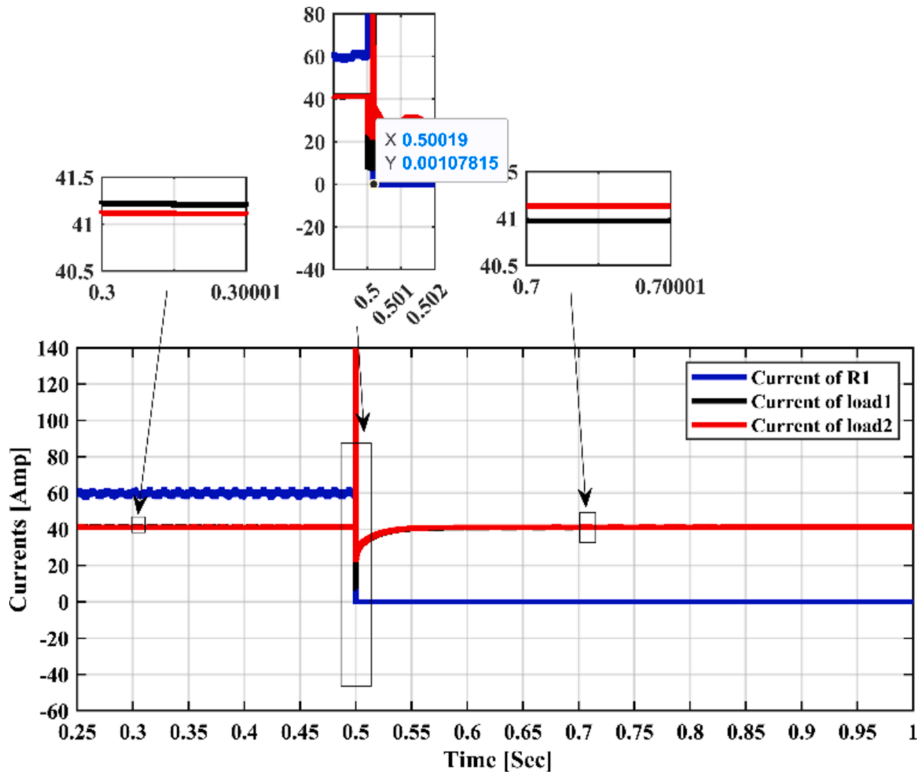


Fig. 6. System currents at F1.

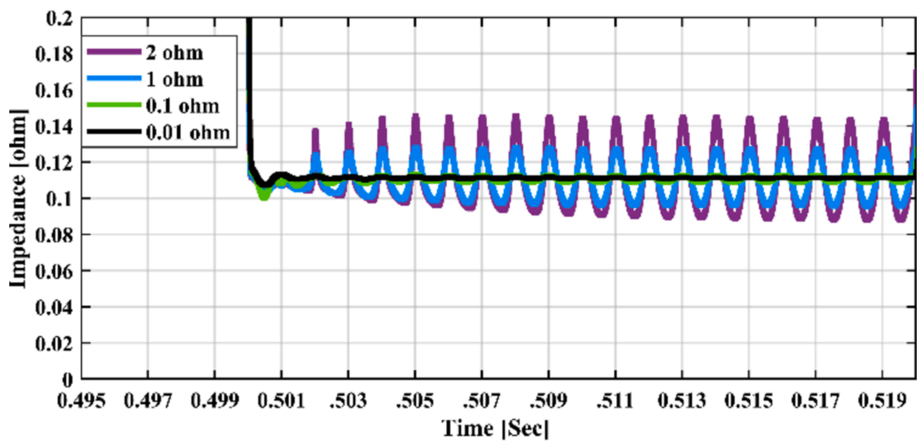


Fig. 7. Estimated impedances at R5 for different fault resistances.

For the protection scheme, the tripping signal from the PC to the relays is delivered depending on the Modbus TCP/IP communication protocol, and the smart meter sends the measured data to the Acti9 SmartLink through the RS485 communication protocol. The experimental platform of this experiment is shown in Fig. 18.

In this practical work, two scenarios are applied, and the results are analyzed. The first scenario is performed to detect faults at different locations of the line. The second one is performed to assess the performance of the proposed approach in the presence of system uncertainties. Load variations and line outages can represent system uncertainties. The following sections will thoroughly explain these scenarios and case studies.

A. Scenario#1 Faults at different locations of a line.
B. Scenario#2 Performance evaluation in the presence of system uncertainties

Case#1 Impact of the Load Variations.
Case#2 Impact of line outage (System Contingency).

***A. Scenario 1: Faults at different locations of a line*.**

In this experiment, a pole-pole solid fault is initiated at different positions along the line between R1 and R2. The fault points are set at 25 %, 50 %, and 75 % of the line. Figs. 19 to 21 illustrate these three cases' corresponding line currents and voltages. In the case of the fault initiated at 25 % of the line (referred to as F1 in Fig. 16), Fig. 19 (a) displays the fault point voltage. While Fig. 19 (b) illustrates the line current. The proposed technique effectively identifies, localizes, and promptly clears the fault within 44 ms. In the case of the fault initiated at 50 % of the line (referred to as F2 in Fig. 16), Fig. 20 (a) illustrates the fault point voltage, while Fig. 20 (b) shows the current of R1. The proposed technique clears the fault within 45 ms. Similarly, in the case of the fault initiated at 75 % of the line (referred to as F3 in Fig. 16), Fig. 21 (a) depicts the fault point voltage, and Fig. 21 (b) displays the current of

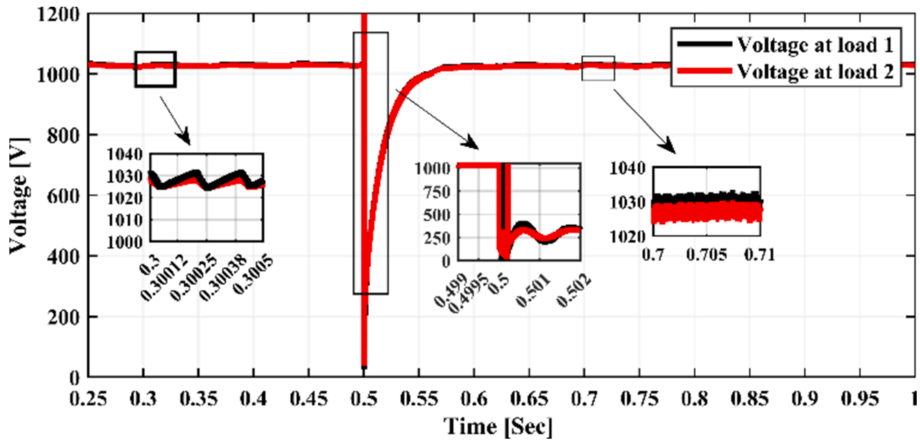


Fig. 8. System voltages during P-P fault at scenario 3 (at t = 0.5 s).

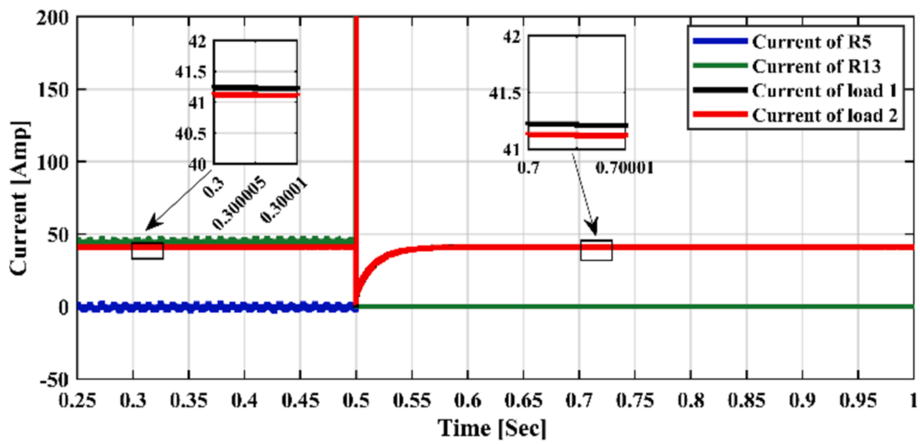


Fig. 9. System currents at scenario 3.

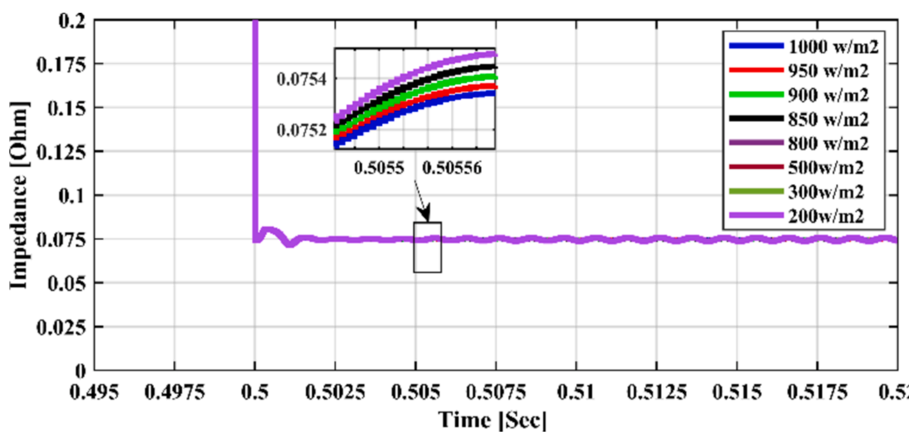


Fig. 10. Estimated impedances at R12 during generation variations.

R1. In this scenario, the fault is successfully cleared within 45 ms. The experimental outcomes unequivocally substantiate the accuracy and efficiency of the proposed approach in precisely detecting and pinpointing faults at distinct positions along the line.

B. Scenario 2: Performance evaluation in the presence of system uncertainties.

In this section, the influence of system uncertainties on the proposed method's performance will be evaluated practically through two case studies. The first is the impact of the load variations and the second is the impact of line outage.

Case#1: Impact of the Load Variations.

The performance of conventional protection techniques during load variations is limited due to changes in the line power flow that affect the measured impedance, and they cannot distinguish between fault current and sudden load change current. A 30 % decrease in load for zone 1 is assumed to explore the proposed method's performance during load variations. A P-P fault with 0 Ω fault resistance is applied at the line between R1 and R2 (F1, in Fig. 16).

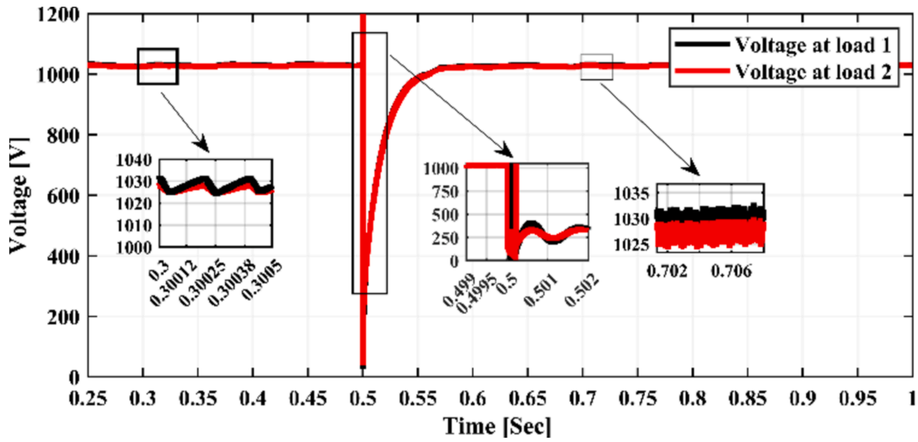


Fig. 11. DC bus voltage during a pole-to-pole fault at F7 (t = 0.5) during load variations.

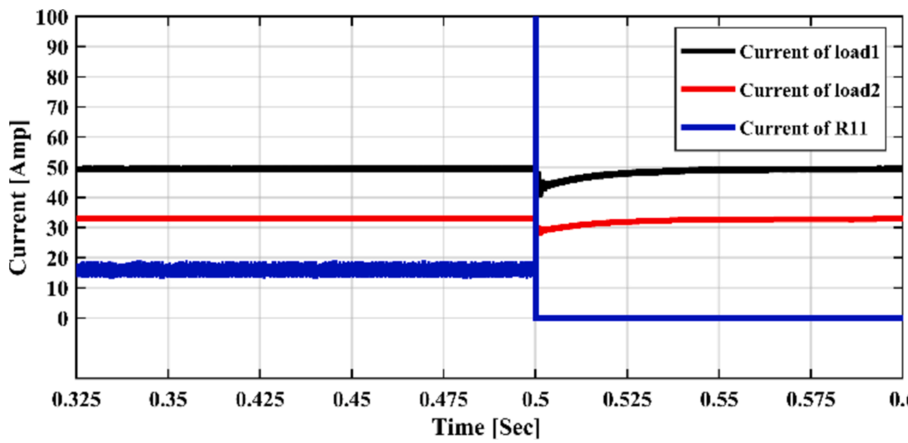


Fig. 12. System currents during load changing.

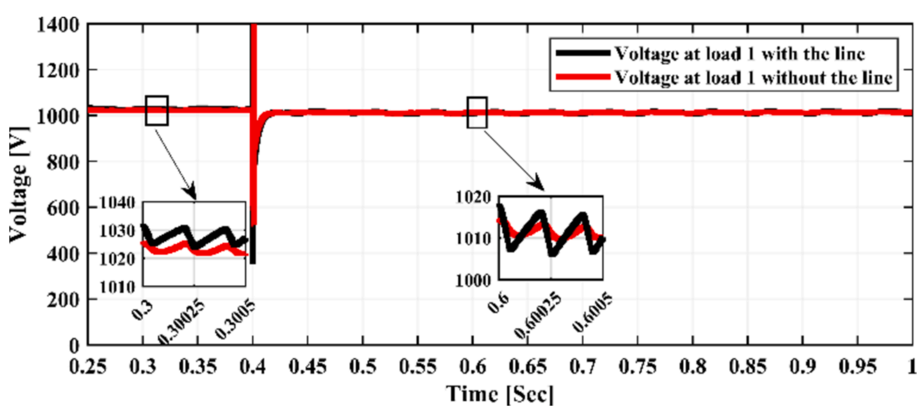


Fig. 13. System voltage with and without the presence of the line between R1 & R2.

The system voltage changes during load variations are shown in Fig. 22 (a). Whereas Fig. 22 (b) shows the line current. However, when the line current is decreased to 10 A, the fault is cleared within 33 ms. These findings demonstrate the enhanced performance and effectiveness of the proposed method in fault detection and clearance, particularly under challenging conditions involving load variations.

Case#2: Impact of Line Outage (System Contingency).

To investigate how the performance of the proposed method is affected by line outages, a solid P-P fault is applied to the line midpoint (at F2, as shown in Fig. 16). The outage is implemented by removing the line between R3 and R4. The effect of this fault on the system is analyzed, and the outcomes are presented in Fig. 23, where Fig. 23 (a) shows the fault point voltage, indicating the system voltage without removing the line between R3 and R4. Whereas Fig. 23 (b) illustrates the corresponding line current when the line is removed. The proposed method effectively detects and clears faults within a time frame of 40 ms. The results underscore its fault detection and localization efficacy, especially in line outages. In comparison, conventional methods show limitations in detecting faults under such circumstances.

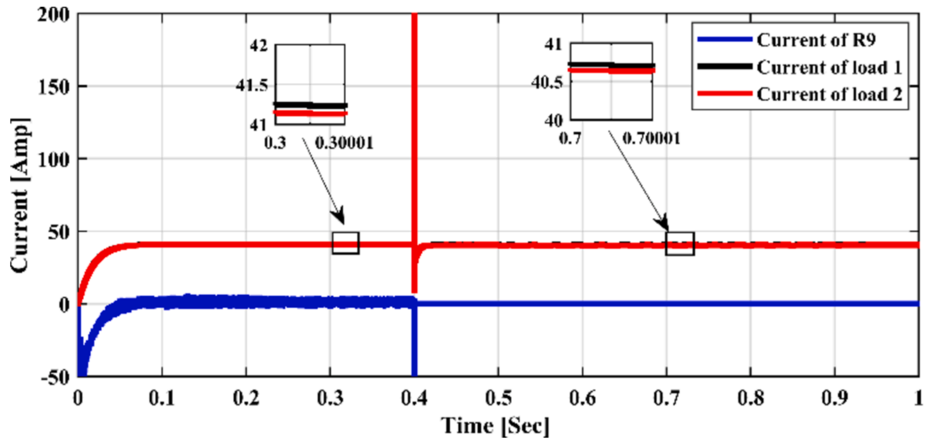


Fig. 14. System currents in case the line between R1 & R2 is absent.

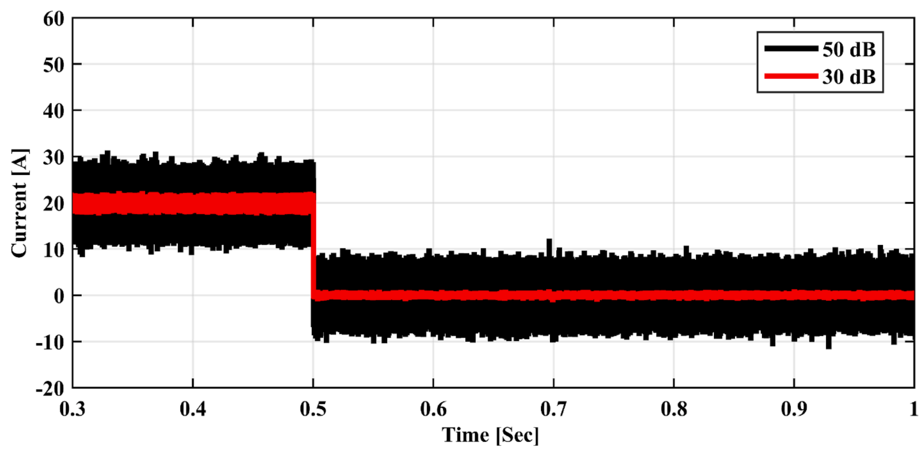


Fig. 15. Currents in the line between R5 & R6 at F2 with different SNR.

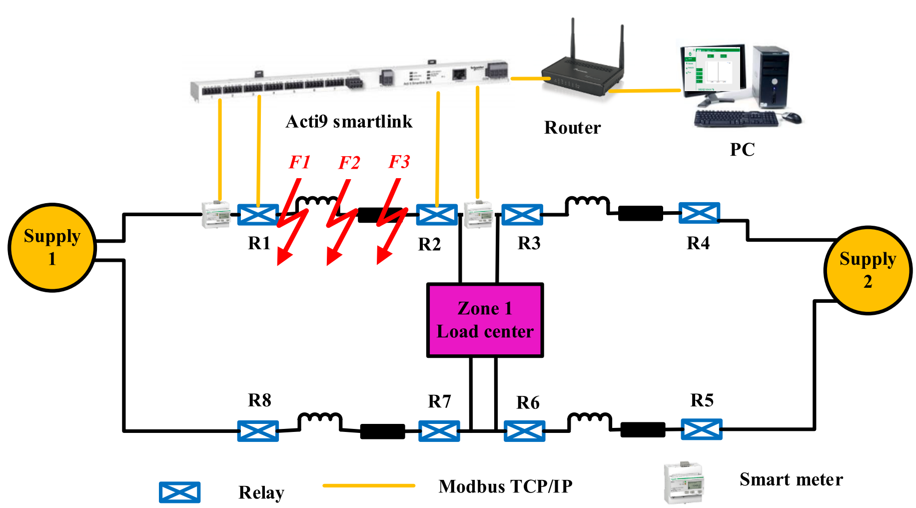


Fig. 16. The architecture of the system illustration.

5. Conclusion

This paper presented a novel protection scheme for zonal shipboard microgrids based on high-frequency impedance estimation, using an intelligent electronic device integrated with the IEC 61850 standard. The method was rigorously validated through both simulation and practical hardware experiments. The key findings are:

- The proposed method achieves highly accurate fault detection, clearing faults within 0.17 ms in simulations and 33–45 ms in hardware testing.

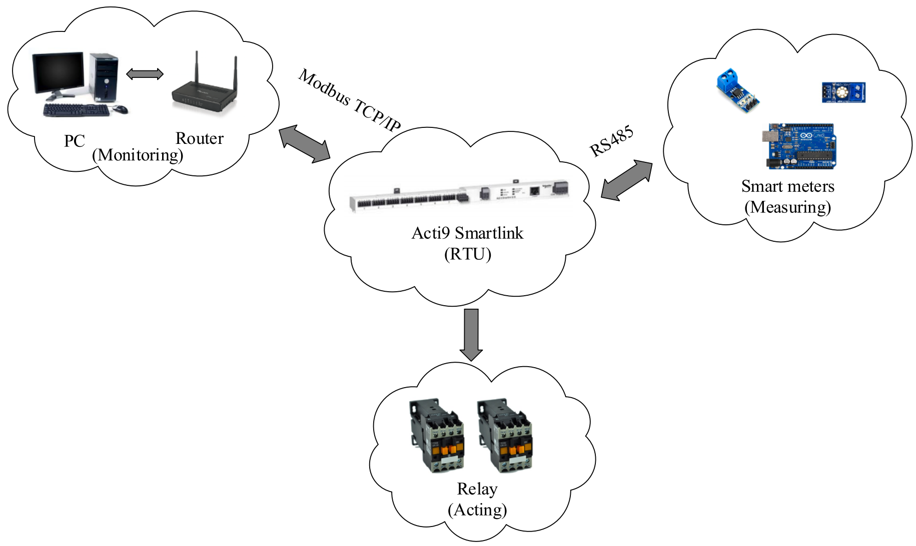


Fig. 17. Main groups of experimental components.

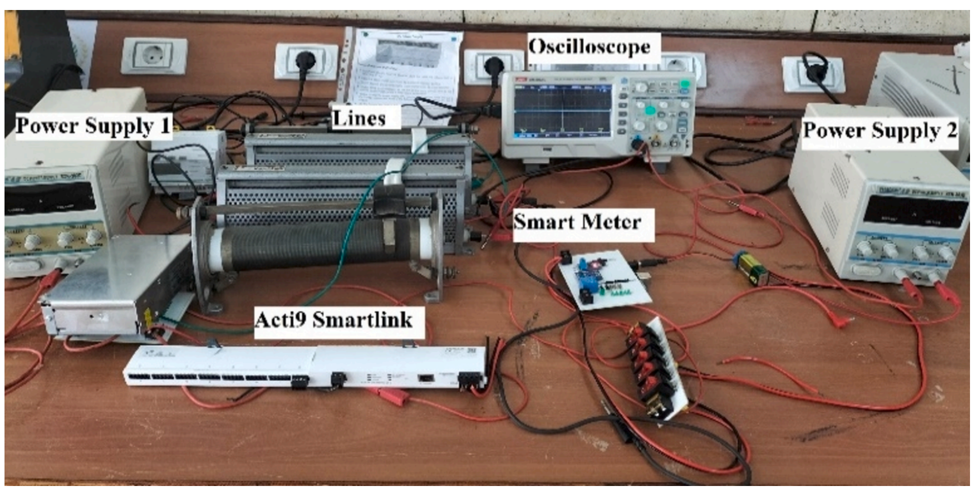


Fig. 18. The experimental testbed.

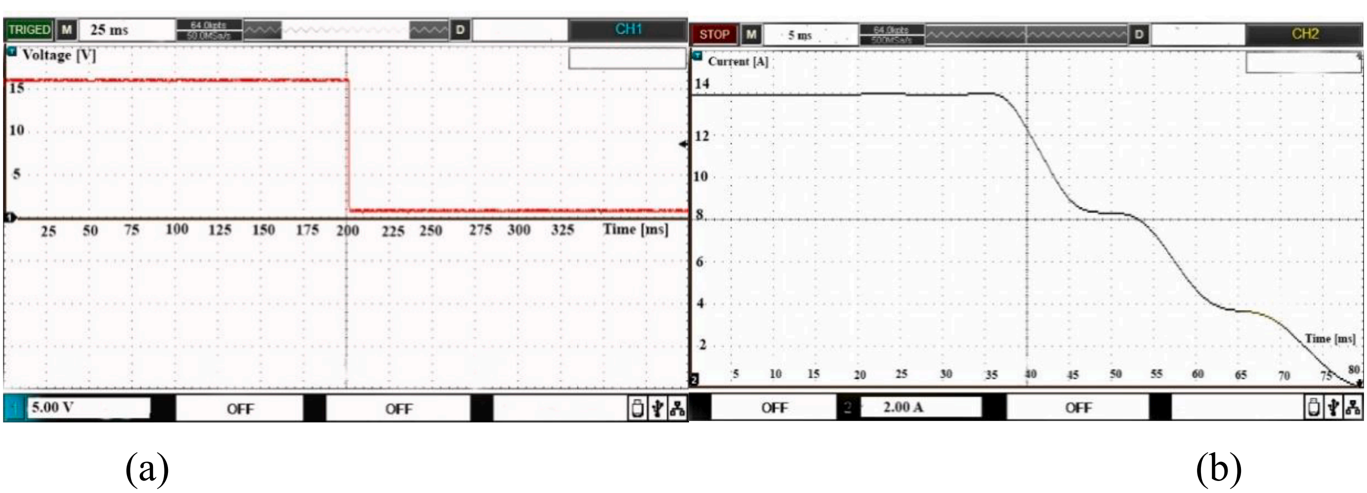
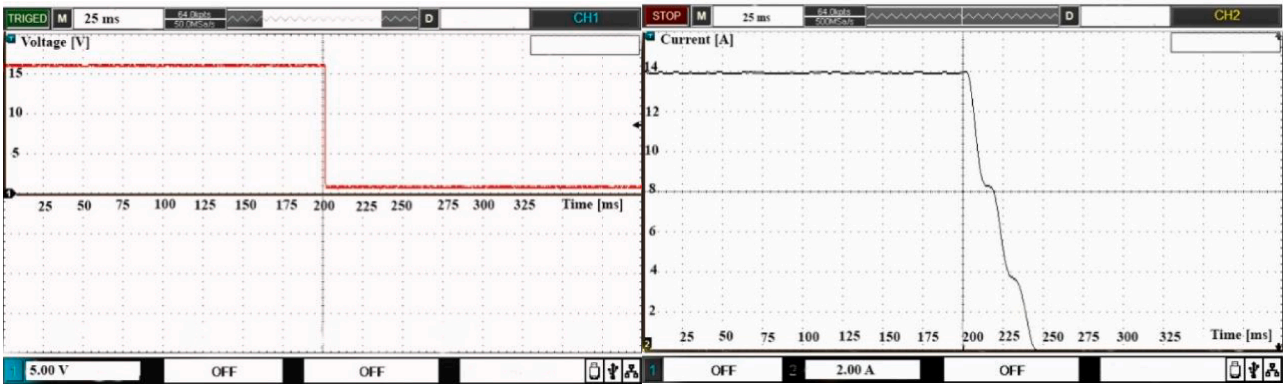
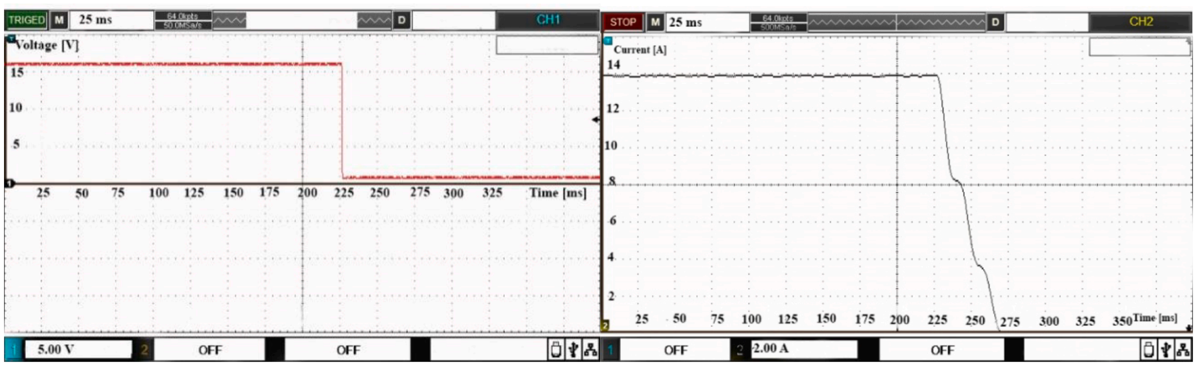


Fig. 19. The experimental outcomes for 25% line fault. (a) Voltage at fault location. (b) Current of R1.



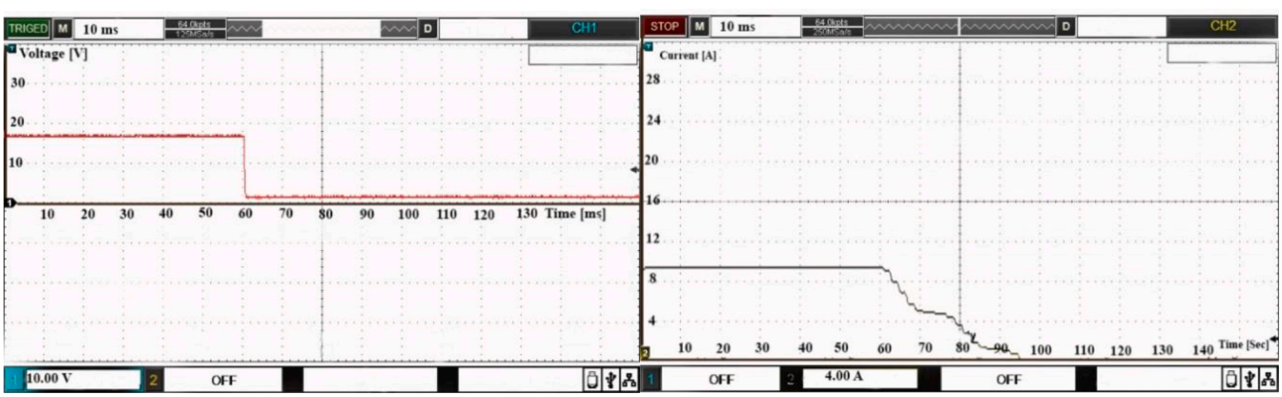
(a) (b)

Fig. 20. The experimental outcomes for 50% line fault. (a) Voltage at fault location. (b) Current of R1.



(a) (b)

Fig. 21. The experimental outcomes for 75% line fault. (a) Voltage at fault location. (b) Current of R1.



(a) (b)

Fig. 22. The experimental outcomes for a fault introduced in case of load variations. (a) Voltage at fault location. (b) Current of R1.

- The approach demonstrated robustness across diverse conditions, including variations in fault resistance, load, generation, and system contingencies, maintaining impedance estimation errors below 5 % for high fault resistances up to 2 Ω.
- Noise immunity was demonstrated under varying SNR ratios (50 dB to 30 dB).
- Hardware experiments confirmed the method's effectiveness even under system uncertainties, such as load variations and simultaneous faults.

These results demonstrate the proposed approach's reliability and applicability for enhancing fault detection in complex, real-world shipboard microgrid environments.

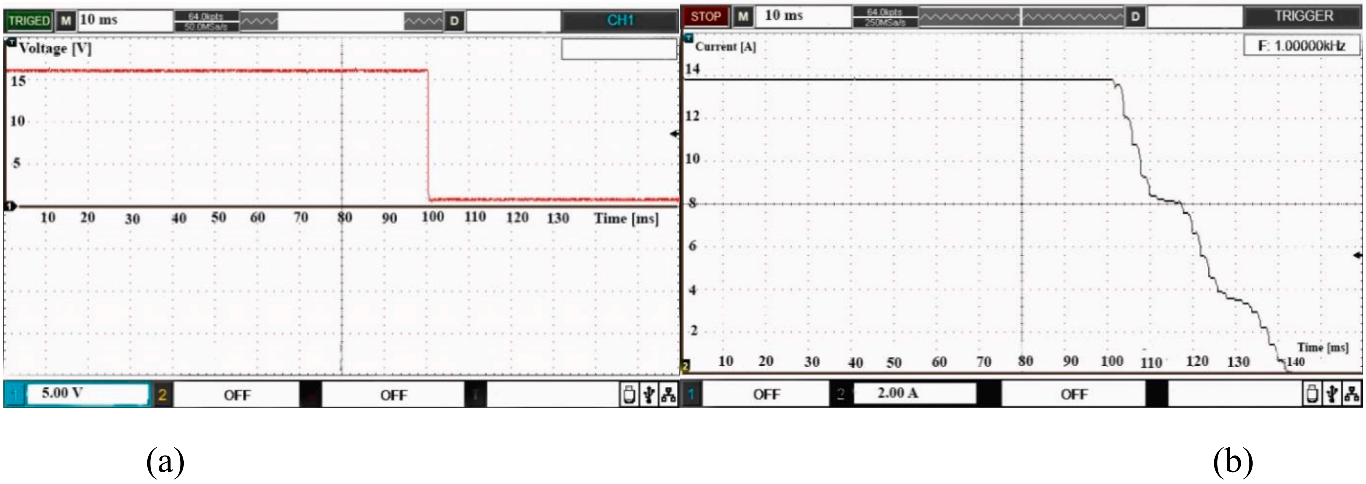


Fig. 23. The experimental outcomes for a fault introduced in case of line outage. (a) Voltage at fault location. (b) Current of R1.

CRediT authorship contribution statement

Asmaa M. Aboelezz: Writing – original draft, Validation, Investigation, Conceptualization. **Magdi M. El-Saadawi:** Visualization, Resources, Investigation, Formal analysis. **Abdelfattah A. Eladl:** Writing – review & editing, Supervision, Methodology, Investigation, Conceptualization. **Magda I. El-Afifi:** Writing – original draft, Resources, Investigation, Formal analysis. **Vladimír Bureš:** Writing – review & editing, Supervision, Project administration, Funding acquisition. **Bishoy E. Sedhom:** Writing – review & editing, Validation, Supervision, Project administration, Methodology.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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